TENTATIVE TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

64 GBIT (8G × 8 BIT) CMOS NAND E^2PROM (Multi-Level-Cell)

DESCRIPTION

The TC58NVG6D2 is a single 3.3 V 64 Gbit (74,594,648,064 bits) NAND Electrically Erasable and Programmable Read-Only Memory (NAND E²PROM) organized as (8192 + 640) bytes × 256 pages × 4124 blocks.
The device has two 8832-byte static registers which allow program and read data to be transferred between the register and the memory cell array in 8832-byte increments. The Erase operation is implemented in a single block unit (2 Mbytes + 160 Kbytes: 8832 bytes × 256 pages).

The TC58NVG6D2 is a serial-type memory device which utilizes the I/O pins for both address and data input/output as well as for command inputs. The Erase and Program operations are automatically executed making the device most suitable for applications such as solid-state file storage, voice recording, image file memory for still cameras and other systems which require high-density non-volatile memory data storage.

FEATURES

- Organization

	TC58NVG6D2G
Memory cell array	8832 × 512K × 8
Register	8832 × 8
Page size	8832 bytes
Block size	(2M + 160 K) bytes

- Modes
  Read, Reset, Auto Page Program, Auto Block Erase, Status Read, Page Copy,
  Multi Page Program, Multi Block Erase, Multi Page Copy, Multi Page Read

- Mode control
  Serial input/output
  Command control

- Number of valid blocks
  Min 3996 blocks
  Max 4124 blocks

- Power supply
  V_{CC} = 2.7 V to 3.6 V

- Access time

Cell array to register	200 μs max
Serial Read Cycle	25 ns min

- Program/Erase time

Auto Page Program	1400 μs/page typ.
Auto Block Erase	5 ms/block typ.

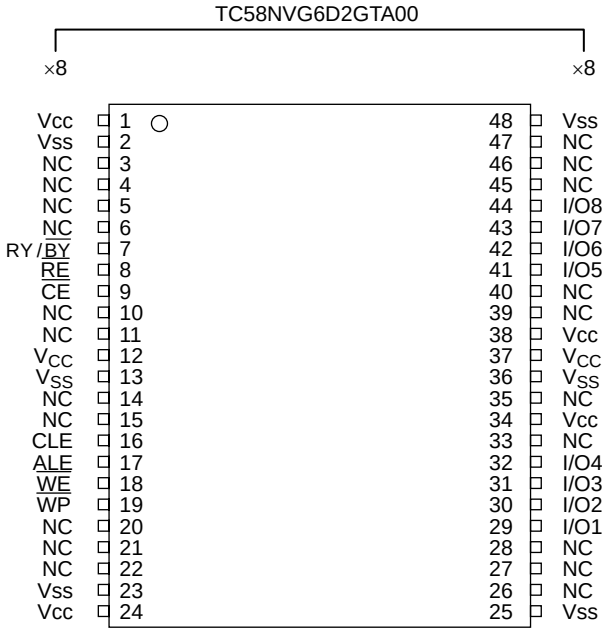
- Operating current

Read (25 ns cycle)	TBD (30 mA max.)
Program (avg.)	TBD (30 mA max.)
Erase (avg.)	TBD (30 mA max.)
Standby	50 μA max

- Package
  (Weight: TBD g typ.)

- FOR RELIABILITY GUIDANCE, PLEASE REFER TO THE APPLICATION NOTES AND COMMENTS (17).

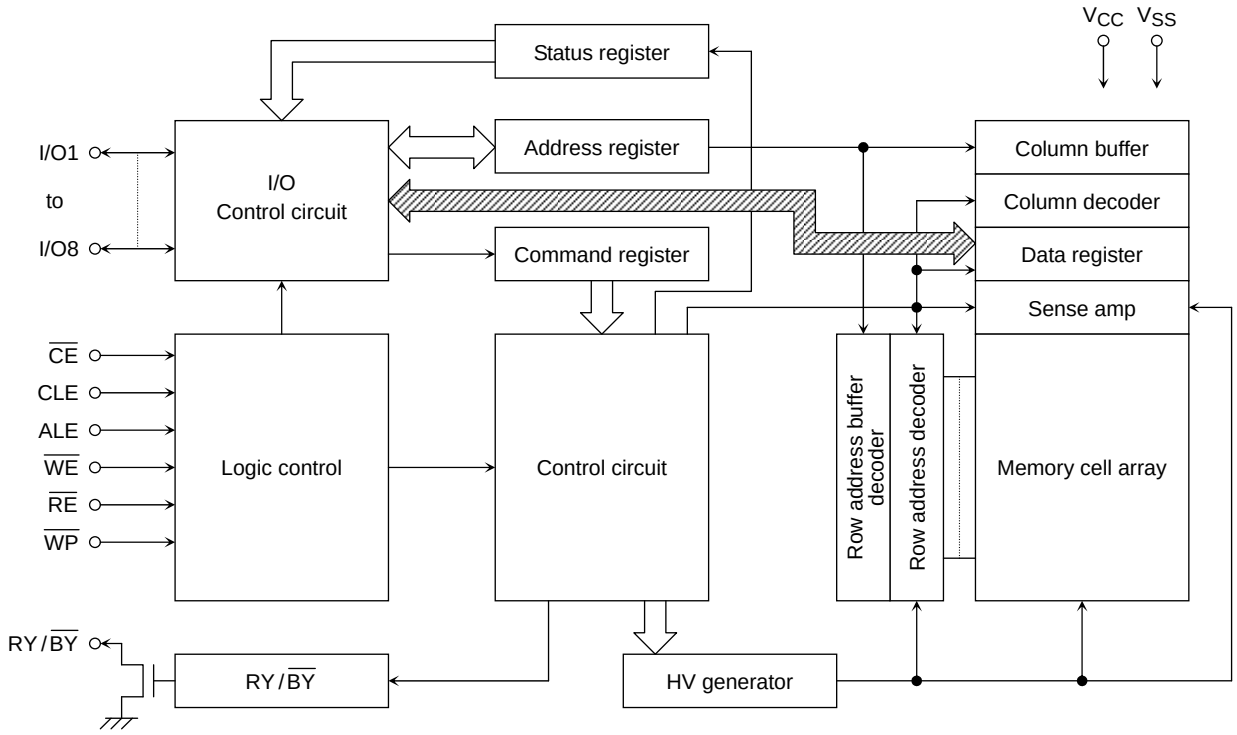
PIN ASSIGNMENT (TOP VIEW)



PIN NAMES

I/O1 ~ I/O8	I/O port
$\overline{CE}$	Chip enable
$\overline{WE}$	Write enable
$\overline{RE}$	Read enable
CLE	Command latch enable
ALE	Address latch enable
$\overline{WP}$	Write protect
RY/$\overline{BY}$	Ready/Busy
V_{CC}	Power supply
V_{SS}	Ground
N.C	No connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
V_{CC}	Power Supply Voltage	−0.6 to 4.6	V
V_{IN}	Input Voltage	−0.6 to 4.6	V
$V_{I/O}$	Input /Output Voltage	−0.6 V to V_{CC} + 0.3 V (≤ 4.6 V)	V
P_D	Power Dissipation	0.3	W
T_{SOLDER}	Soldering Temperature (10 s)	260	°C
T_{STG}	Storage Temperature	-55 to 150	°C
T_{OPR}	Operating Temperature	0 to 70	°C

CAPACITANCE *(Ta = 25°C, f = 1 MHz)

SYMB0L	PARAMETER	CONDITION	MIN	MAX	UNIT
C_{IN}	Input	V_{IN} = 0 V	—	10	pF
C_{OUT}	Output	V_{OUT} = 0 V	—	10	pF

* This parameter is periodically sampled and is not tested for every device.

VALID BLOCKS

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT
N_{VB}	Number of Valid Blocks	3996	—	4124	Blocks

NOTE: The device occasionally contains unusable blocks. Refer to Application Note (13) toward the end of this document.
The first block (Block 0) is guaranteed to be a valid block at the time of shipment.
The specification for the minimum number of valid blocks is applicable over the device lifetime.
* The number of valid blocks includes extended blocks.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER		MIN	TYP.	MAX	UNIT
V_{CC}	Power Supply Voltage		2.7 V	—	3.6 V	V
V_{IH}	High Level input Voltage	2.7 V ≤ V_{CC} ≤ 3.6 V	0.8 x Vcc	—	V_{CC} + 0.3	V
V_{IL}	Low Level Input Voltage	2.7 V ≤ V_{CC} ≤ 3.6 V	–0.3*	—	0.2 x Vcc	V

* –2 V (pulse width lower than 20 ns)

DC CHARACTERISTICS (Ta = 0 to 70°C, V_{CC} = 2.7 V to 3.6 V)

SYMBOL	PARAMETER	CONDITION	MIN	TYP.	MAX	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0 V to V_{CC}	—	—	±10	μA
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to V_{CC}	—	—	±10	μA
I_{CCO0} *1	Power On Reset Current	$\overline{CE}$ = V_{IL}	—	—	TBD	mA
I_{CCO1} *2	Serial Read Current(Single page)	$\overline{CE}$ = V_{IL}, I_{OUT} = 0 mA, tcycle = 25 ns	—	—	TBD	mA
	Serial Read Current(Multi-page)	$\overline{CE}$ = V_{IL}, I_{OUT} = 0 mA, tcycle = 25 ns	—	—	TBD	mA
I_{CCO2} *2	Programming Current(Single page)	—	—	—	TBD	mA
	Programming current(Multi-page)	—	—	—	TBD	mA
I_{CCO3}	Single Block Erasing current	—	—	—	TBD	mA
	Multi-block Erasing current	—	—	—	TBD	mA
I_{CCS}	Standby Current	$\overline{CE}$ = V_{CC} – 0.2 V, $\overline{WP}$ = 0 V/V_{CC},	—	—	50	μA
V_{OH}	High Level Output Voltage	I_{OH} = –0.4 mA (2.7 V ≤ V_{CC} ≤ 3.6 V)	2.4	—	—	V
V_{OL}	Low Level Output Voltage	I_{OL} = 2.1 mA (2.7 V ≤ V_{CC} ≤ 3.6 V)	—	—	0.4	V
I_{OL} ($R\overline{Y}/\overline{BY}$)	Output current of $R\overline{Y}/\overline{BY}$ pin	V_{OL} = 0.4 V (2.7 V ≤ V_{CC} ≤ 3.6 V)	—	8	—	mA

*1: Icco0 is the average current during R/B signal="Busy" state.

*2: All operation current are without data cache.

AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

(Ta = 0 to 70°C, V_{CC} = 2.7 V to 3.6 V)

SYMBOL	PARAMETER	MIN	MAX	UNIT
t_{CLS}	CLE Setup Time	10	—	ns
t_{CLS2}	CLE Setup Time	40	—	ns
t_{CLH}	CLE Hold Time	5	—	ns
t_{CS}	$\overline{CE}$ Setup Time	20	—	ns
t_{CS2}	$\overline{CE}$ Setup Time	32	—	ns
t_{CH}	$\overline{CE}$ Hold Time	5	—	ns
t_{WP}	Write Pulse Width	12	—	ns
t_{ALS}	ALE Setup Time	10	—	ns
t_{ALH}	ALE Hold Time	5	—	ns
t_{DS}	Data Setup Time	10	—	ns
t_{DH}	Data Hold Time	5	—	ns
t_{WC}	Write Cycle Time	25	—	ns
t_{WH}	$\overline{WE}$ High Hold Time	10	—	ns
t_{WHW} *	$\overline{WE}$ High Hold Time from final address to first data	300	—	ns
t_{WW}	$\overline{WP}$ High to $\overline{WE}$ Low	100	—	ns
t_{RR}	Ready to $\overline{RE}$ Falling Edge	20	—	ns
t_{RW}	Ready to $\overline{WE}$ Falling Edge	20	—	ns
t_{RP}	Read Pulse Width	12	—	ns
t_{RC}	Read Cycle Time	25	—	ns
t_{REA}	$\overline{RE}$ Access Time	—	20	ns
t_{CR}	$\overline{CE}$ Low to $\overline{RE}$ Low	10	—	ns
t_{CLR}	CLE Low to $\overline{RE}$ Low	10	—	ns
t_{AR}	ALE Low to $\overline{RE}$ Low	10	—	ns
t_{RHOH}	Data Output Hold Time from $\overline{RE}$ High	25	—	ns
t_{RLOH}	Data Output Hold Time from $\overline{RE}$ Low	5	—	ns
t_{RHZ}	$\overline{RE}$ High to Output High Impedance	—	60	ns
t_{CHZ}	$\overline{CE}$ High to Output High Impedance	—	30	ns
t_{CLHZ}	CLE High to Output High Impedance	—	30	ns
t_{REH}	$\overline{RE}$ High Hold Time	10	—	ns
t_{IR}	Output-High-impedance-to-$\overline{RE}$ Falling Edge	0	—	ns
t_{RHW}	$\overline{RE}$ High to $\overline{WE}$ Low	30	—	ns
t_{WHC}	$\overline{WE}$ High to $\overline{CE}$ Low	30	—	ns
t_{WHR1}	$\overline{WE}$ High to $\overline{RE}$ Low (Status Read)	180	—	ns
t_{WHR2}	$\overline{WE}$ High to $\overline{RE}$ Low (Column Address Change in Read)	300	—	ns
t_{R}	Memory Cell Array to Starting Address	—	200	µs
$t_{DCBSYR1}$	Data Cache Busy in Read Cache (following 31h and 3Fh)	—	200	µs
$t_{DCBSYR2}$	Data Cache Busy in Page Copy (following 3Ah)	—	205	µs
t_{WB}	$\overline{WE}$ High to Busy	—	100	ns
t_{RST}	Device Reset Time (Ready/Read/Program/Erase)	—	10/10/30/100	µs

* tWHW is the time from the $\overline{WE}$ rising edge of final address cycle to the $\overline{WE}$ falling edge of first data cycle.

AC TEST CONDITIONS

PARAMETER	CONDITION
	2.7 V ≤ V_{CC} ≤ 3.6 V
Input level	0 V to V_{CC}
Input pulse rise and fall time	3ns
Input comparison level	V_{CC}/2
Output data comparison level	V_{CC}/2
Output load	C_L (50 pF) + 1 TTL

Note: Busy to ready time depends on the pull-up resistor tied to the RY/$\overline{BY}$ pin.
(Refer to Application Note (9) toward the end of this document.)

PROGRAMMING AND ERASING CHARACTERISTICS

(Ta = 0 to 70°C, V_{CC} = 2.7 V to 3.6 V)

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT	NOTES
t_{PROG}	Average Programming Time	—	1400	2400	μs	
$t_{DCBSYW1}$	Data Cache Busy Time in Write Cache (following 11h)	—	0.5	1	μs	
$t_{DCBSYW2}$	Data Cache Busy Time in Write Cache (following 15h)	—	—	2400	μs	(2)
N	Number of Partial Program Cycles in the Same Page	—	—	—		(1)
t_{BERASE}	Block Erasing Time	—	5	10	ms	

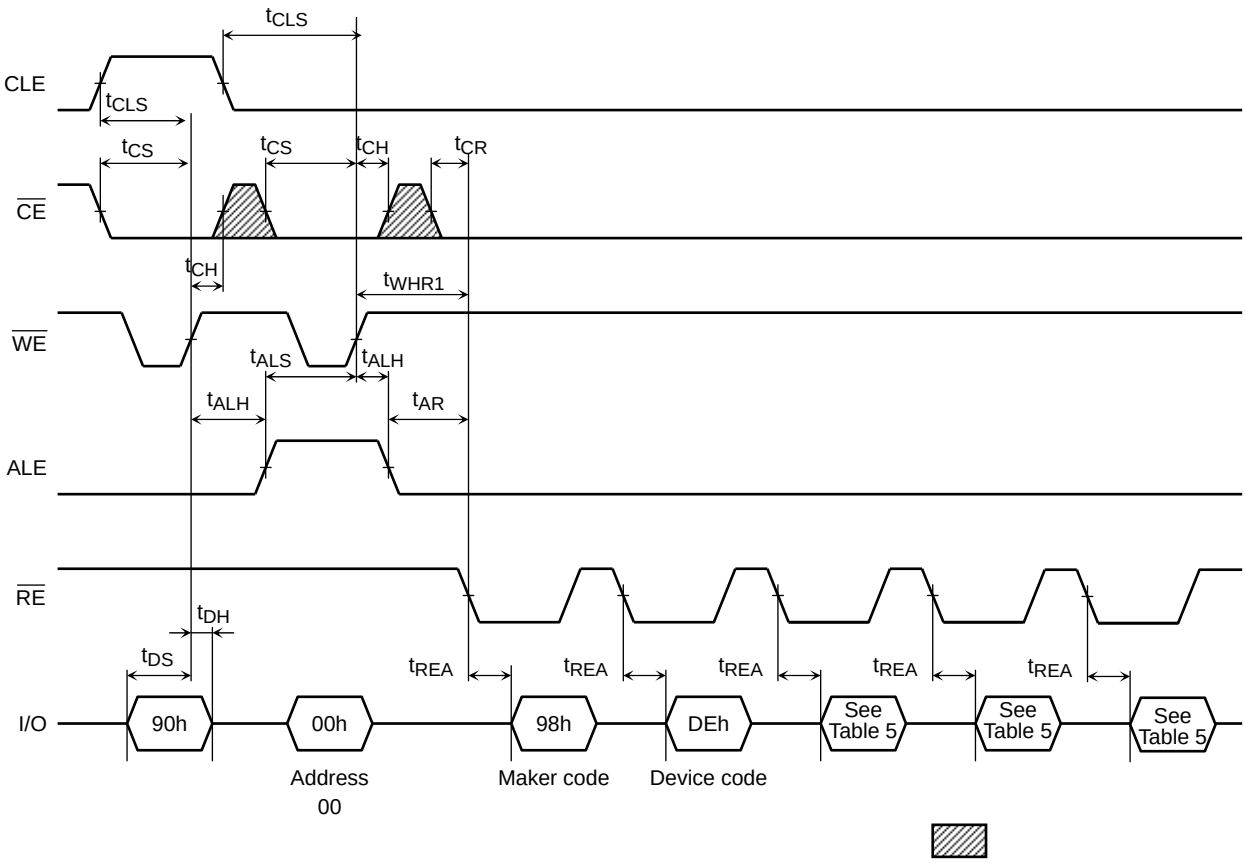
(1) Refer to Application Note (12) toward the end of this document.

(2) $t_{DCBSYW2}$ depends on the timing between internal programming time and data in time.

Data Output

When tREH is long, output buffers are disabled by /RE=High, and the hold time of data output depend on tRHOH (25 ns MIN). On this condition, waveforms look like normal serial read mode.
When tREH is short, output buffers are not disabled by /RE=High, and the hold time of data output depend on tRLOH (5ns MIN). On this condition, output buffers are disabled by the rising edge of CLE, ALE, /CE or falling edge of /WE, and waveforms look like Extended Data Output Mode.

ID Read Operation Timing Diagram



PIN FUNCTIONS

The device is a serial access memory which utilizes time-sharing input of address information.

Command Latch Enable: CLE

The CLE input signal is used to control loading of the operation mode command into the internal command register. The command is latched into the command register from the I/O port on the rising edge of the $\overline{WE}$ signal while CLE is High.

Address Latch Enable: ALE

The ALE signal is used to control loading address information into the internal address register. Address information is latched into the address register from the I/O port on the rising edge of $\overline{WE}$ while ALE is High.

Chip Enable: $\overline{CE}$

The device goes into a low-power Standby mode when $\overline{CE}$ goes High during the device is in Ready state. The $\overline{CE}$ signal is ignored when device is in Busy state ($RY/\overline{BY}$ = L), such as during a Program or Erase or Read operation, and will not enter Standby mode even if the $\overline{CE}$ input goes High.

Write Enable: $\overline{WE}$

The $\overline{WE}$ signal is used to control the acquisition of data from the I/O port.

Read Enable: $\overline{RE}$

The $\overline{RE}$ signal controls serial data output. Data is available t_{REA} after the falling edge of $\overline{RE}$.
The internal column address counter is also incremented (Address = Address + 1) on this falling edge.

I/O Port: I/O1 to 8

The I/O1 to 8 pins are used as a port for transferring address, command and input/output data to and from the device.

Write Protect: $\overline{WP}$

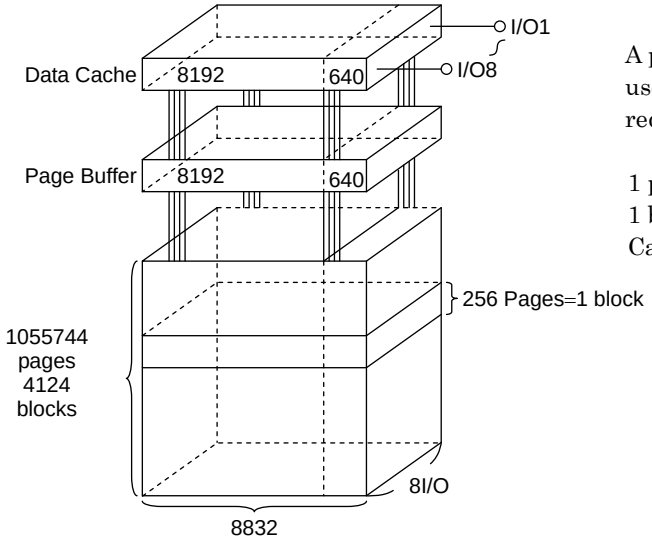
The $\overline{WP}$ signal is used to protect the device from accidental programming or erasing. The internal voltage regulator is reset when $\overline{WP}$ is Low. This signal is usually used for protecting the data during the power-on/off sequence when input signals are invalid.

Ready/Busy: $RY/\overline{BY}$

The $RY/\overline{BY}$ output signal is used to indicate the operating condition of the device. The $RY/\overline{BY}$ signal is in Busy state ($RY/\overline{BY}$ = L) during the Program, Erase and Read operations and will return to Ready state ($RY/\overline{BY}$ = H) after completion of the operation. The output buffer for this signal is an open drain and has to be pulled-up to Vcc with an appropriate resister.

Schematic Cell Layout and Address Assignment

The Program operation works on page units while the Erase operation works on block units.



A page consists of 8832 bytes in which 8192 bytes are used for main memory storage and 640 bytes are for redundancy or for other uses.

1 page = 8832 bytes
1 block = 8832 bytes × 256 pages = (2M + 160K) bytes
Capacity = 8832 bytes × 256 pages × 4124 blocks

Table 1. Addressing

	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1
First cycle	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
Second cycle	L	L	CA13	CA12	CA11	CA10	CA9	CA8
Third cycle	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Fourth cycle	PA15	PA14	PA13	PA12	PA11	PA10	PA9	PA8
Fifth cycle	L	L	L	PA20	PA19	PA18	PA17	PA16

CA0 to CA13: Column address
PA0 to PA20: Page address

PA8 to PA20: Block address
PA0 to PA7: NAND address in block

Extended Blocks Arrangement

The device has 28 extended blocks to increase valid blocks. Extended blocks can be accessed by the following addressing.

Page Address(PA0-20)	64Gbits	
00000h	Block 0(District 0)	Main Blocks (4096 blocks)
00100h	Block 1(District 1)	
00200h	Block 2(District 0)	
00300h	Block 3(District 1)	
00400h	Block 4(District 0)	
00500h	Block 5(District 1)	
|	|	
FFE00h	Block 4094(District 0)	
FFF00h	Block 4095(District 1)	
100000h	Block 4096(District 0)	Extended Blocks (28 blcoks)
100100h	Block 4097(District 1)	
|	|	
101A00h	Block 4122(District 0)	
101B00h	Block 4123(District 1)	
101C00h – FFFFFFh	**Address Gap**	

ID Read

The device contains ID codes which can be used to identify the device type, the manufacturer, and features of the device. The ID codes can be read out under the following timing conditions:

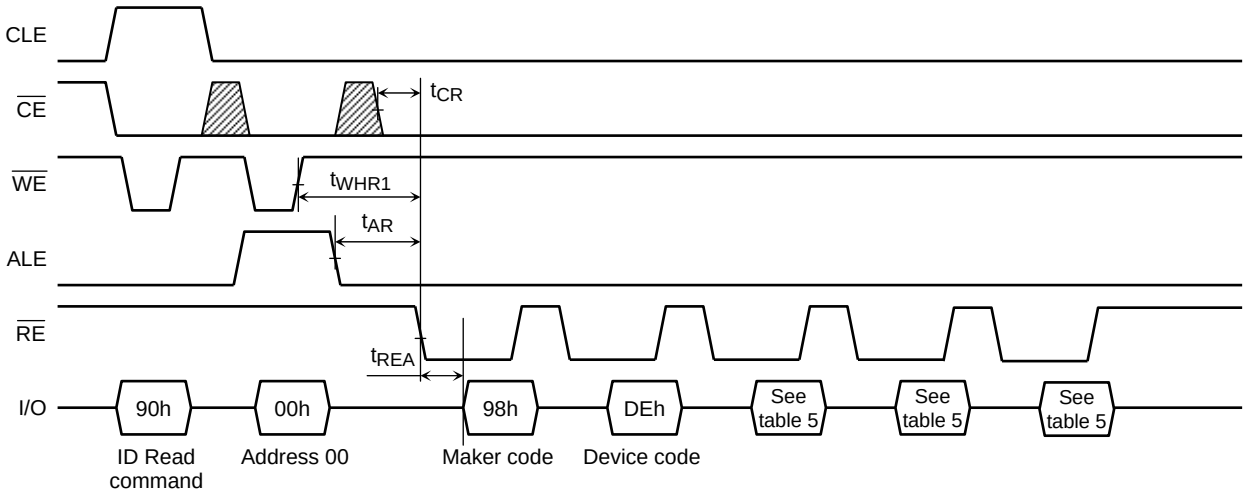


Table 5. Code table

	Description	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	Hex Data
1st Data	Maker Code	1	0	0	1	1	0	0	0	98h
2nd Data	Device Code	1	1	0	1	1	1	1	0	DEh
3rd Data	Chip Number, Cell Type	—	—	—	—	—	—	—	—	See table
4th Data	Page Size, Block Size	—	—	—	—	—	—	—	—	See table
5th Data	Plane Number	—	—	—	—	—	—	—	—	See table

3rd Data

	Description	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1
Internal Chip Number	1 2 4 8							0 0 1 1	0 1 0 1
Cell Type	2 level cell 4 level cell 8 level cell 16 level cell					0 0 1 1	0 1 0 1		

4th Data

	Description	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1
Page Size (without redundant area)	2 KB							0	0
	4 KB							0	1
	8 KB							1	0
	Reserved							1	1
Block Size (without redundant area)	128 KB	0		0	0				
	256 KB	0		0	1				
	512 KB	0		1	0				
	1 MB	0		1	1				
	2 MB	1		0	0				
	Reserved	1		0	1				
	Reserved	1		1	0				
	Reserved	1		1	1				

5th Data

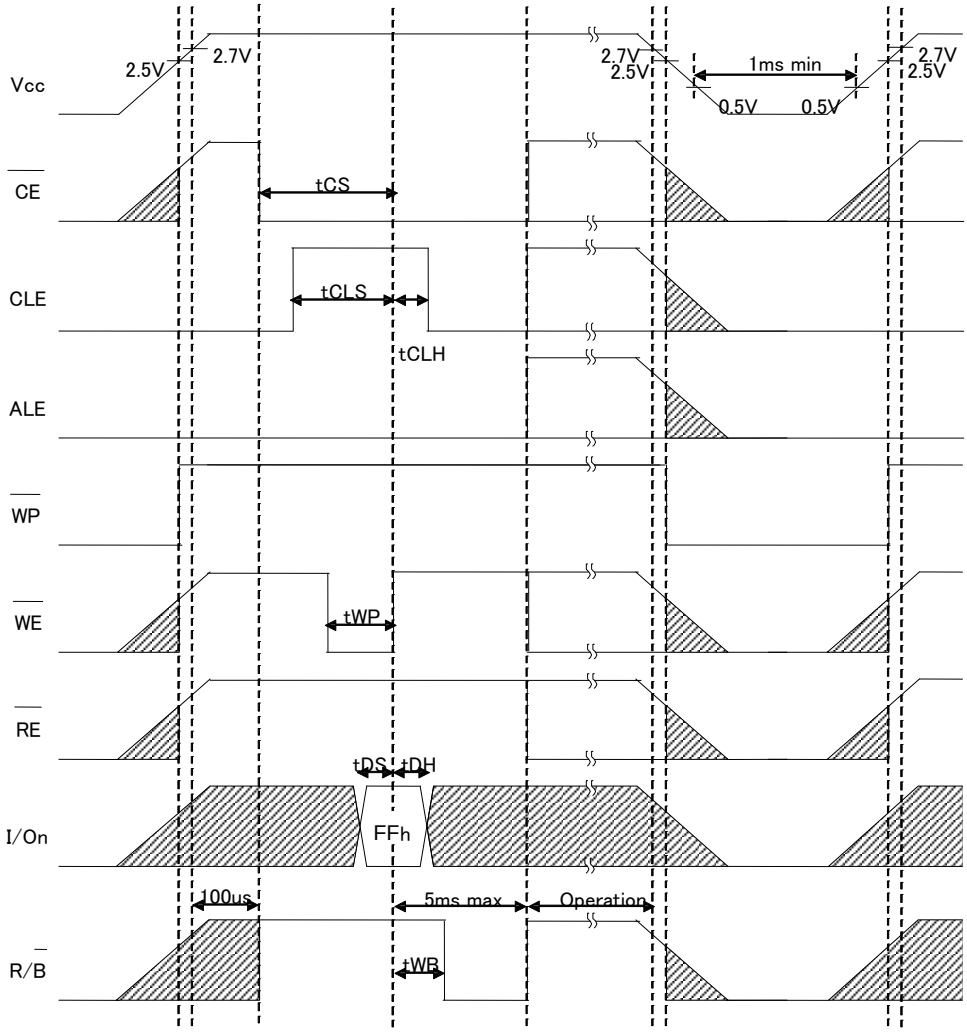
	Description	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1
Plane Number	1 Plane					0	0		
	2 Plane					0	1		
	4 Plane					1	0		
	8 Plane					1	1		

APPLICATION NOTES AND COMMENTS

(1) Power-on/off sequence

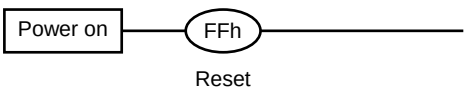
Power-on/off sequence are necessary to follow the timing sequence shown in the figure below. The device internal initialization starts with FFh command after the power supply reaches an appropriate level and wait 100us. During the initialization, the device RY/$\overline{BY}$ signal indicates the Busy state and the device consumes power-on initialize current which is defined on DC characteristics table. The acceptable commands are FFh or 70h(71h/F1h) during this period. The $\overline{WP}$ signal is useful for protecting against data corruption at power-on/off.

During Power-off sequence, when Vcc level is less than 2.5V, Vcc must set below 0.5V and stay 1ms at least.



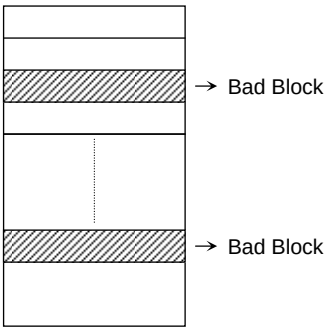
(2) Power-on Reset

The device will not complete its self initialization during power on and will not consume I_{CCO0}, and completes the initialization process with the first Reset command input after power on. During the first FFh reset Busy period, the device consumes a maximum power-on initialize current which is defined on DC characteristics table.



(12) Invalid blocks (bad blocks)

The device occasionally contains unusable blocks. Therefore, the following issues must be recognized:



At the time of shipment, the bad block information is marked on each bad block. Please do not perform an erase operation to bad blocks. It may be impossible to recover the bad block information if the information is erased.

Check if the device has any bad blocks after installation into the system. Refer to the test flow for bad block detection. Bad blocks which are detected by the test flow must be managed as unusable blocks by the system.

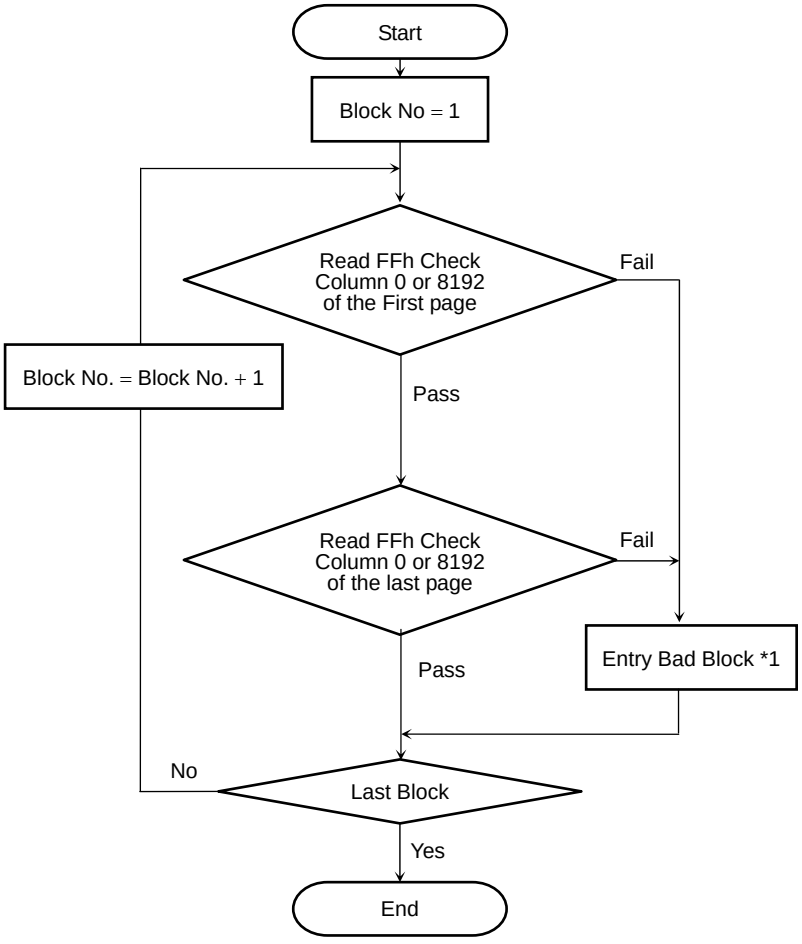
A bad block does not affect the performance of good blocks because it is isolated from the bit lines by select gates.

The number of valid blocks over the device lifetime is as follows:

	MIN	TYP.	MAX	UNIT
Valid (Good) Block Number	3996	—	4124	Block

Bad Block Test Flow

Regarding invalid blocks, bad block mark is in either the 1st or the last page.



*1: No erase operation is allowed to detected bad blocks

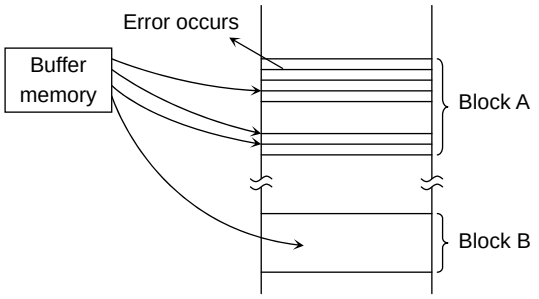
(13) Failure phenomena for Program and Erase operations

The device may fail during a Program or Erase operation.
The following possible failure modes should be considered when implementing a highly reliable system.

FAILURE MODE		DETECTION AND COUNTERMEASURE SEQUENCE
Block	Erase Failure	Status Read after Erase → Block Replacement
Page	Programming Failure	Status Read after Program → Block Replacement
Random Bit	Programming Failure "1 to 0"	ECC

- ECC:TBD.
- Block Replacement

Program



When an error happens in Block A, try to reprogram the data into another Block (Block B) by loading from an external buffer. Then, prevent further system accesses to Block A (by creating a bad block table or by using another appropriate scheme).

Erase

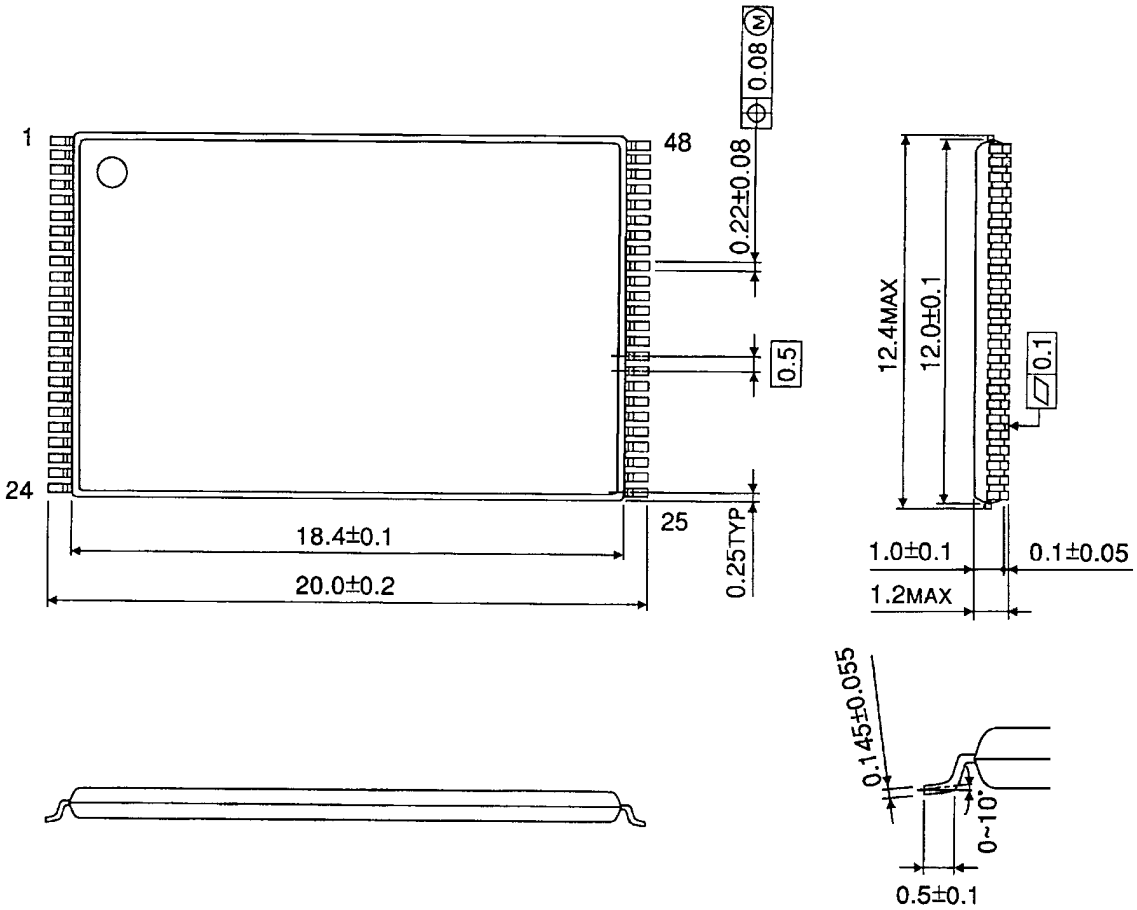
When an error occurs during an Erase operation, prevent future accesses to this bad block (again by creating a table within the system or by using another appropriate scheme).

(14) Do not turn off the power before write/erase operation is complete. Avoid using the device when the battery is low. Power shortage and/or power failure before write/erase operation is complete will cause loss of data and/or damage to data.

(15) If FF reset command is input before completion of write operation to page B, it may cause damage to data not only to the programmed page, but also to the adjacent page A. Regarding page A and B, please see Page 43.

Package Dimensions

TSOP I 48-P-1220-0.50 Unit : mm



Weight: TBD g (typ.)

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